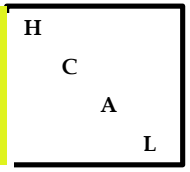
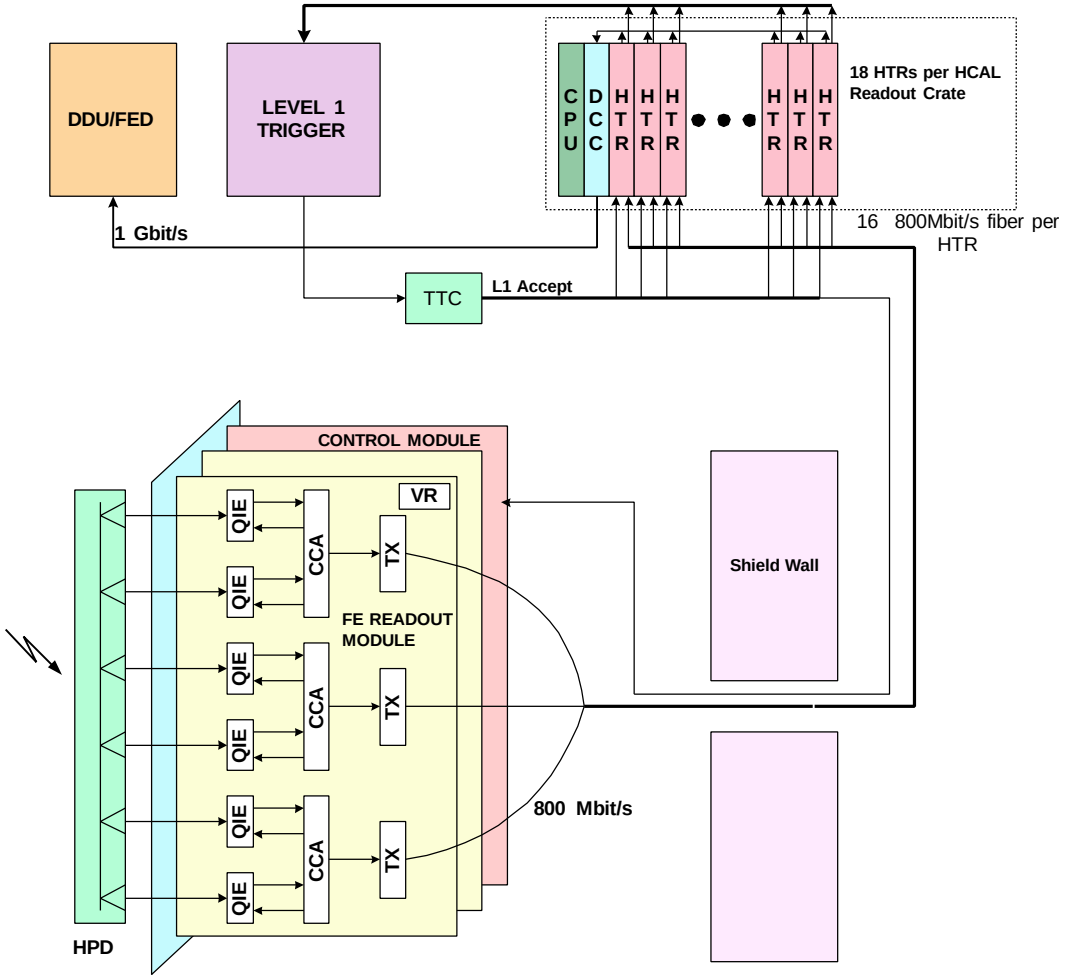
HCAL Front End Electronics



Front End Status

June 2001 CMS Week

FE/DAQ Readout



Pending Issues(1)

Do we instrument Layer 0 ?

- HB, HE RBX design effected
- =>this has stalled HE and HB backplane progress

Dropping Layer 0 results in

- More elegant RBX design - no more HPD-73
- Reduction of channel count and electronics
- Power Savings
- Cost savings of >$850K

Pending Issues(2)

What is the speed of the optical data link?

- **We are examing two possible modes for operating the CERN Gigabit Optical Link (GOL)**
  - 800 Mbps G-Link Protocol
  - 1600 Mbps 8B/10B Protocol
- **Baseline is 800Mbps**
- **Efforts under way at Fermi and Maryland to study faster link**

The link will be the subject of a proposed meeting at Fermilab in a few weeks to understand possible schedule impacts and manpower requirements

Current Work

We have picked a 3U x 160mm format to begin prototype work.

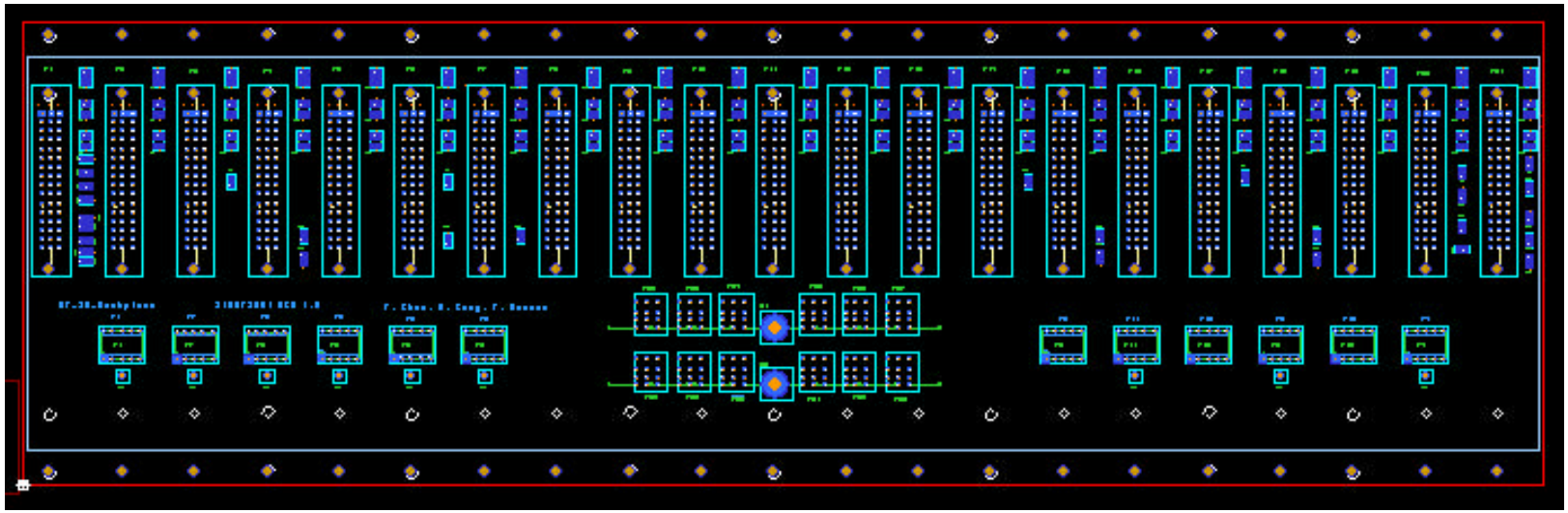
This work includes:

- **The design and production of a 21 slot 3U custom backplane**
- **The design of a clock distribution card which utilizes a TTCrx test board**
- **The design of a two channel FE card which will use bare die QIEs**
- **The design of an RBXbus interface card which can be controlled through a PC**

3U Backplane

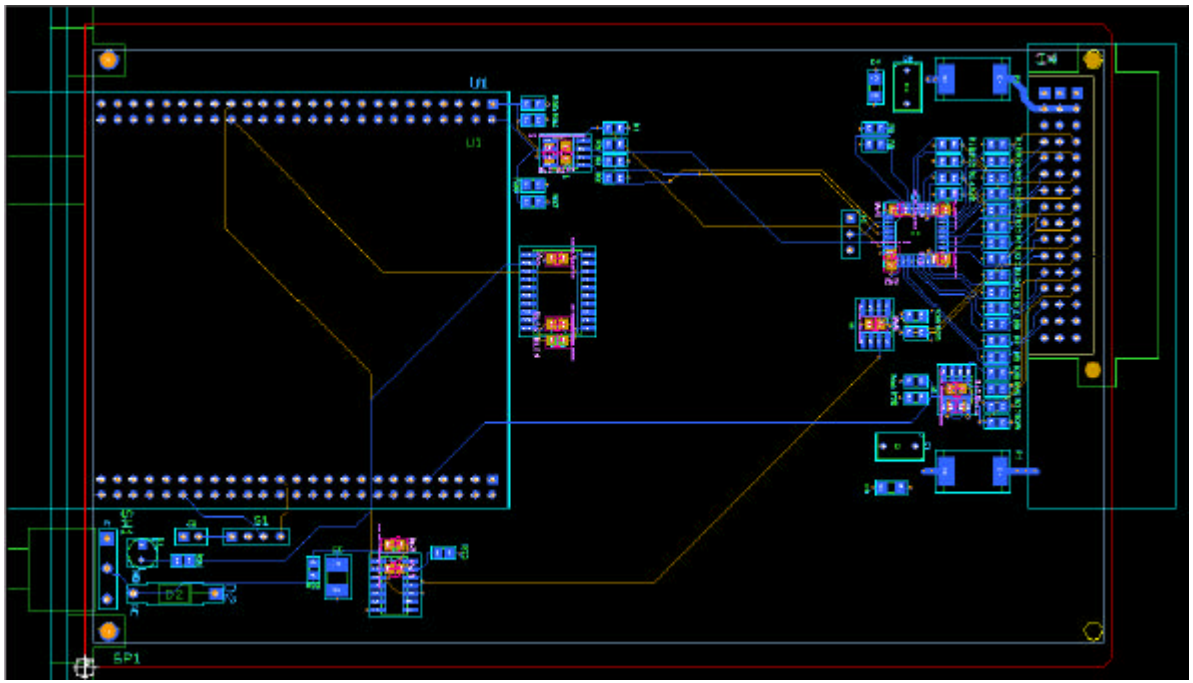
3U backplane is being produced to facilitate prototype work- easy to work with and duplicate

Candidate for HF



Timing Card

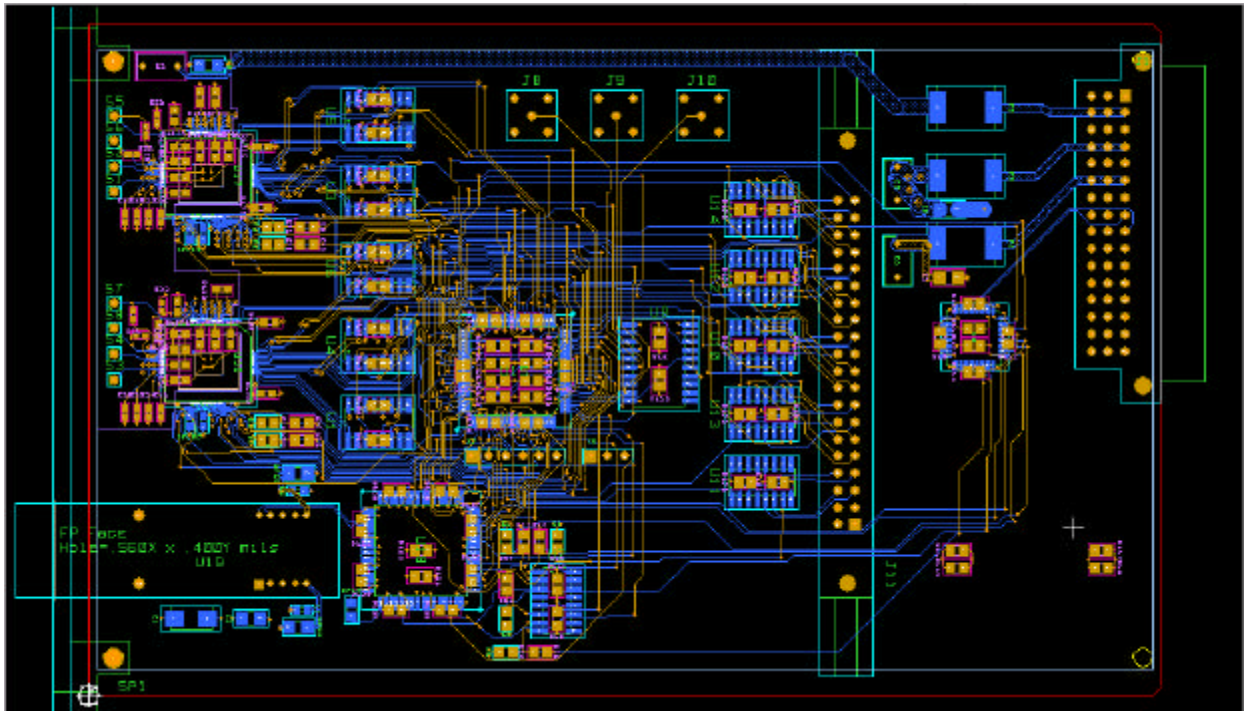
- Will distribute TTCrx clock via LVPECL(note change from LVDS due to rad study results)



FE Proto Ver 1.0

FE Prototype Card

- Will instrument two QIE channels (bare die)
- Data output via G-Link or LVDS copper link



RBXbus Interface Card

- Interface between PC and backplane RBXbus (serial download)

VCSEL Selection(1)

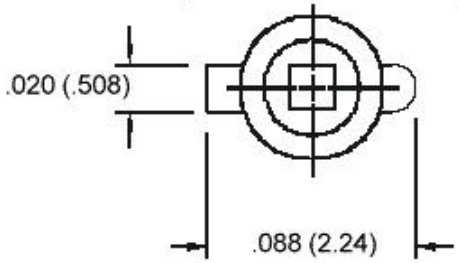
HFE4086-001

VCSEL Components, Data Communications, Flat Window Pillpack, Unattenuate optics, no back monitor photodiode

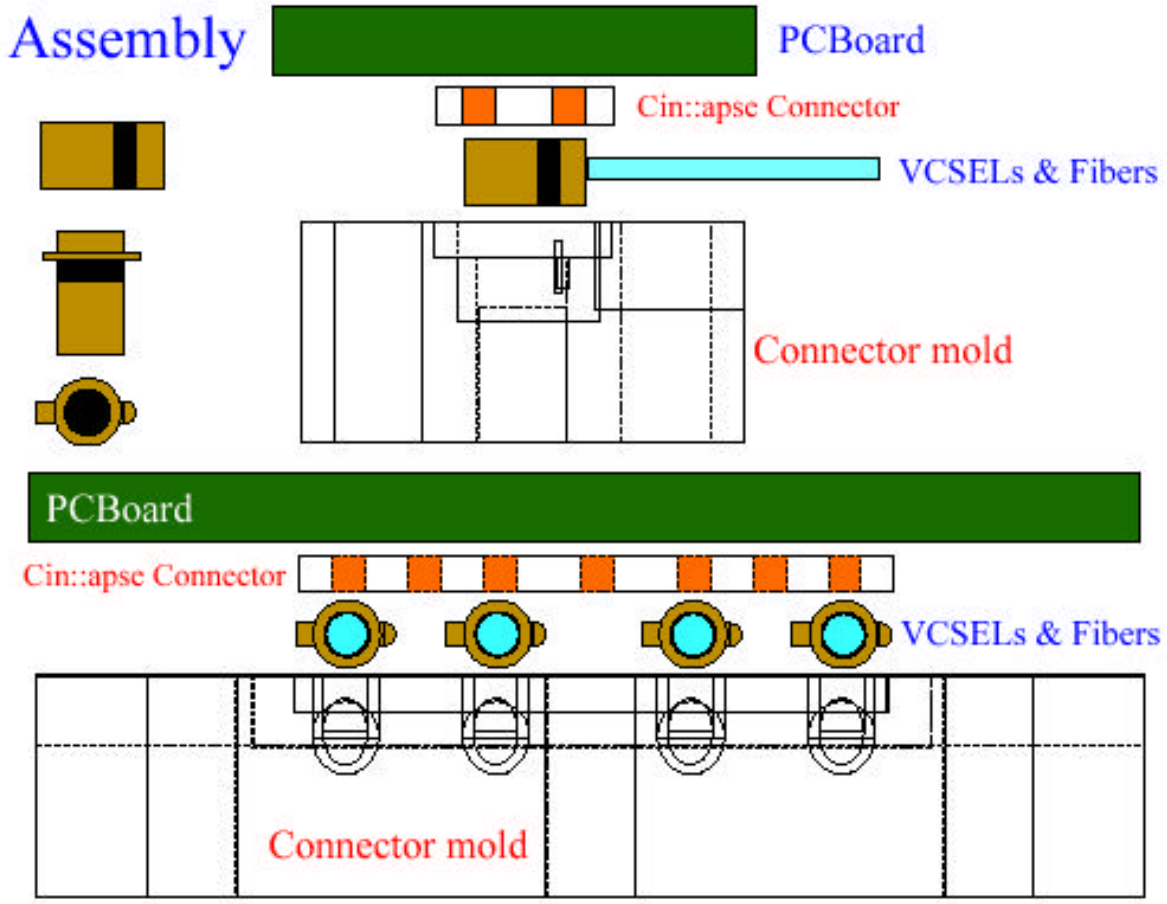
FEATURES

- Designed for drive currents between 5 mA and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz
- Miniature flat-window, pill-pack package

MOUNTING DIMENSIONS (for reference only): in./(mm)



VCSEL Packaging(1)



VCSEL Selection/Packaging(2)

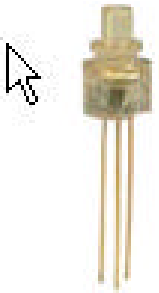
Honeywell

Fiber Optic LAN Components — HFE419x-521

LC Connectorized High Speed VCSEL 2.5 Gbps — *Preliminary*

FEATURES

- Designed for small form factor transceivers
- Prealigned connector sleeve that is compatible with the LC standard (LC is a trademark of Lucent Technologies)
- Designed for drive currents
- Optimized for low dependence of electrical properties over temperature
- High speed ≥1 GHz
- Two different laser/ photodiode polarities
- Attenuating coating
- Packaged with a photodetector



NEW!

The HFE419x-521 is a high-performance 850 nm VCSEL (Vertical Cavity Surface-Emitting Laser) packaged for high-speed data communications. This product combines all the performance advantages of the VCSEL with a custom designed power monitor diode. The power monitor diode can be used with appropriate feedback control circuitry to set a maximum power level for each VCSEL. In addition, built-in power attenuation reduces the effective slope efficiency. These combined features simplify design for high data rate communication and eye safety.

Power Consumption

Power Consumption – NOTE that this is with Layer 0 instrumentation

HB – 298 W
23A@6.5V
33A@4.5V

HE – 205 W
17A@6.5V
21A@4.5V

HO+/- – 135 W
10A@6.5V
15A@4.5V

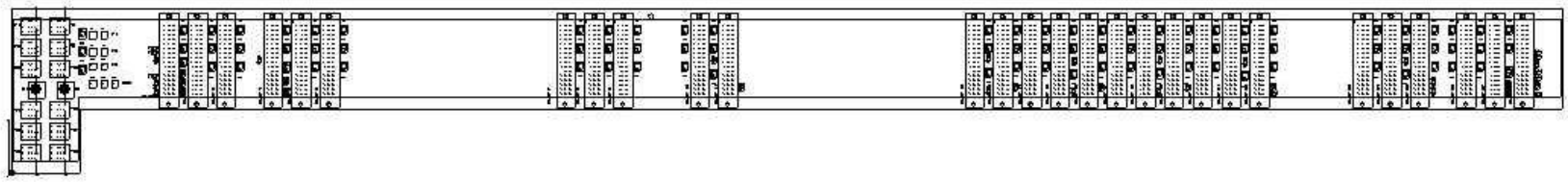
HO-0 – 189 W
16A@6.5V
21A@4.5V

			CURRENT and POWER at BOARD LEVEL										
FE Boards	QTY/BRD			POWER CONSUPTION					IDLING CURRENT				**TOTAL**
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	6		0.2	0.4									
CCA	3					0.3							
Serializer	3				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Board			0.265	0.505		0.897727							
Total Power / Board													**9.044773**
Calibration Module		(There are two boards per module)											
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	3		0.2	0.4									
CCA	3					0.3							
Serializer	2				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Module			0.145	0.265		0.697727							
Total Power / Module													**5.804773**
CCM													
		VOLTAGE				3.3							
Chips						5							
LV regulators													
Current / Board						1.515152							
Total Power / Board													**6.818182**

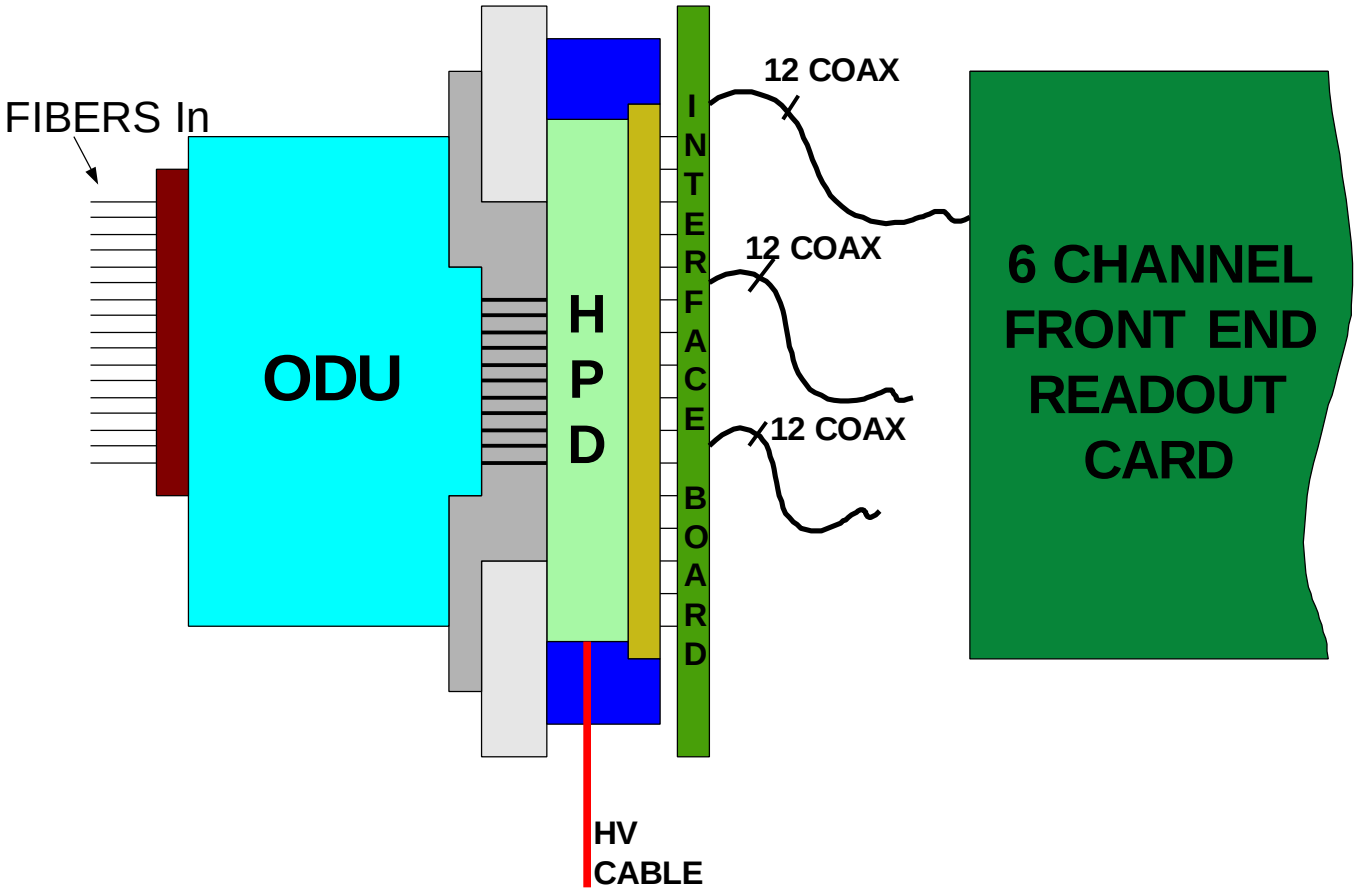
HB Backplane Function

Backplane

- ~87 CM LONG
- Provides Power
- Distributes 40 MHz Clock (3 load max)
- Provides path for RBXbus (serial communication bus)
- Temperature feedback



Readout Module Overview



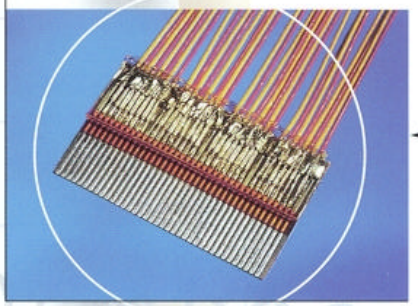
Signal Cable Candidates (1)

H C A L

PICO-FLEX®

OR USE PICO-FLEX :

- Mounted in a ZIF connector surface mounted on a PCB.
- Available in 0,5 mm pitch (0,019").
- Compatible with PICO-COAX® AWG 40 to 46 (50 and 100 pF/m, 15 and 30 pF/ft).
- Custom designed versions available on request.

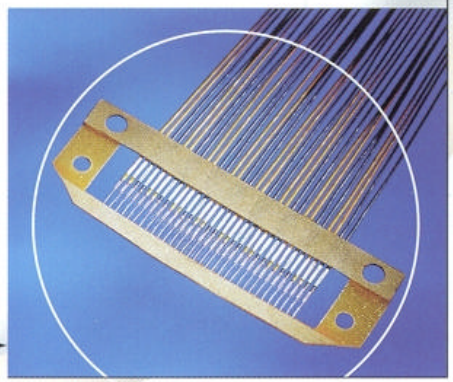


Plug

PICO-WELD®

USE PICO-WELD® :

- Solders directly to PC board.
- Maintains alignment of the PICO-COAX® at a constant pitch.
- Hot bar system soldering.
- Available in 32 positions pitch 0,635 mm (0,025").
- Compatible with AWG 40 and 42 (50 and 100 pF/m, 15 and 30 pF/ft).
- Other constructions available on request



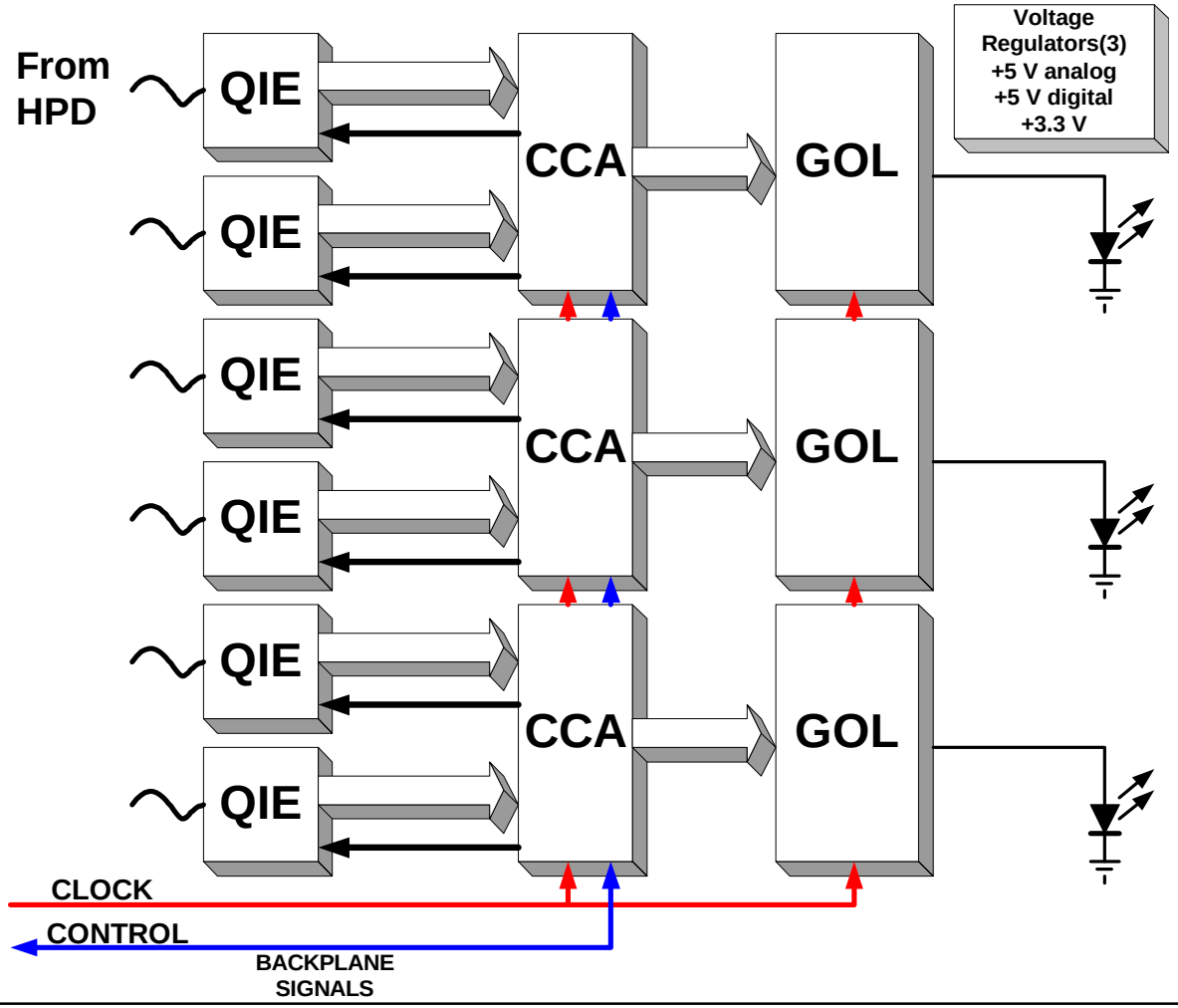
Solder

Signal Cable Candidates (2)

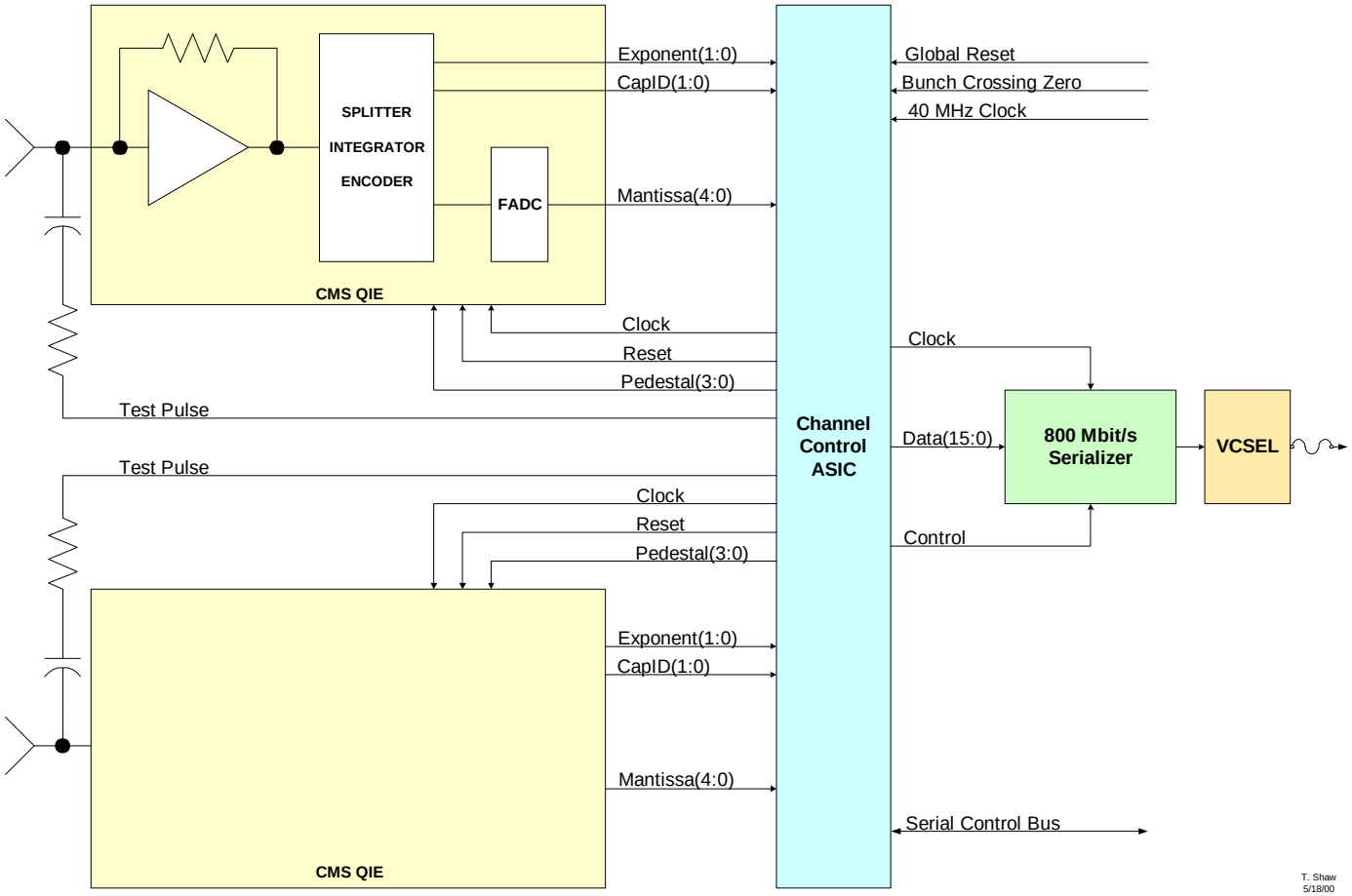
0.5 mm pitch

Cables studies will be made when we receive the first QIE in June

Block Diagram of FE Card



FE Channels



CMS QIE Solution

QIE Description

H C A L

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

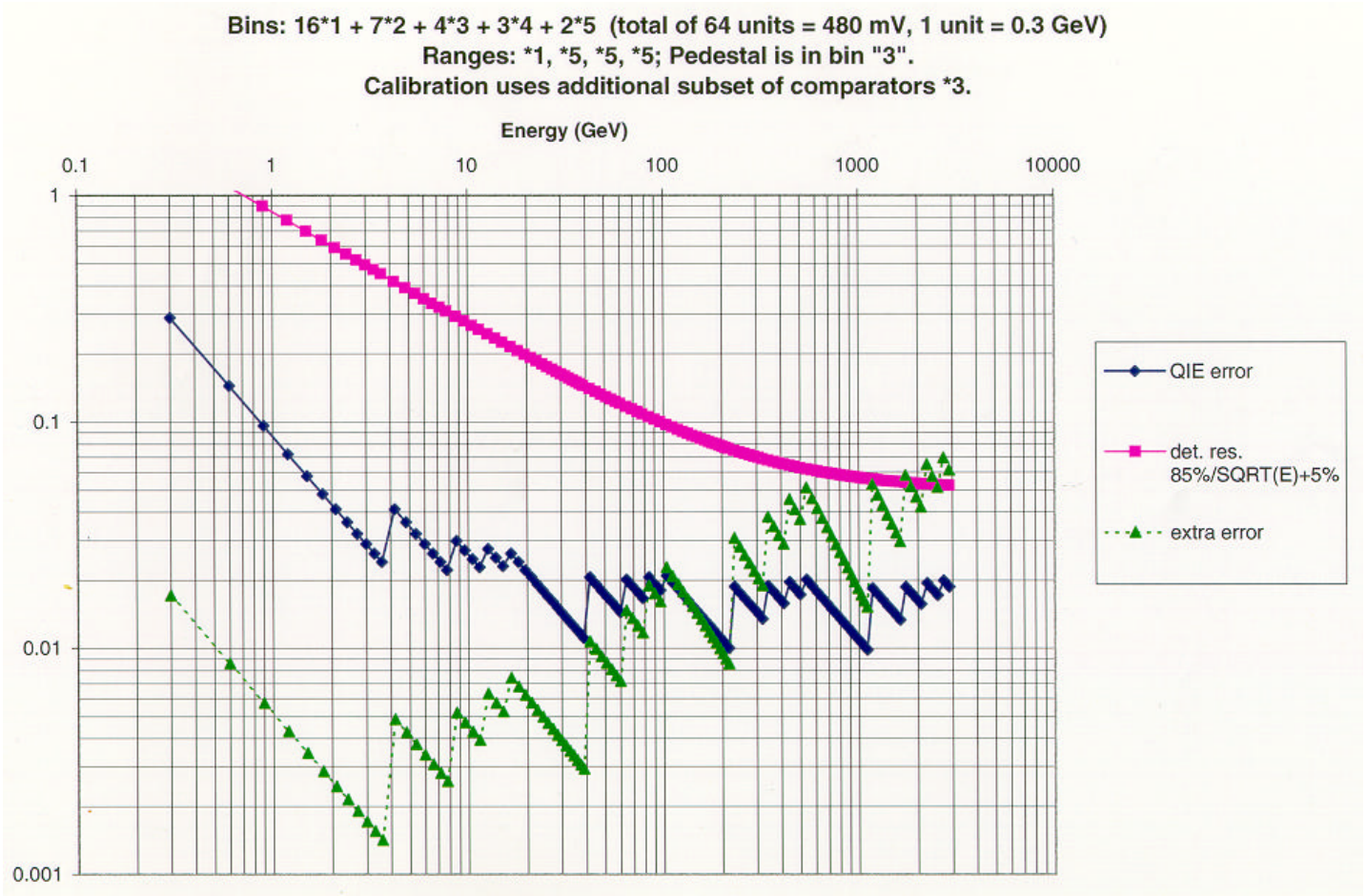
- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

QIE Specification

QIE Design Specifications

- Clock > 40 MHz
- Must have inverting and non-inverting inputs
- Charge sensitivity of lowest range – 1fC/LSB
  - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs

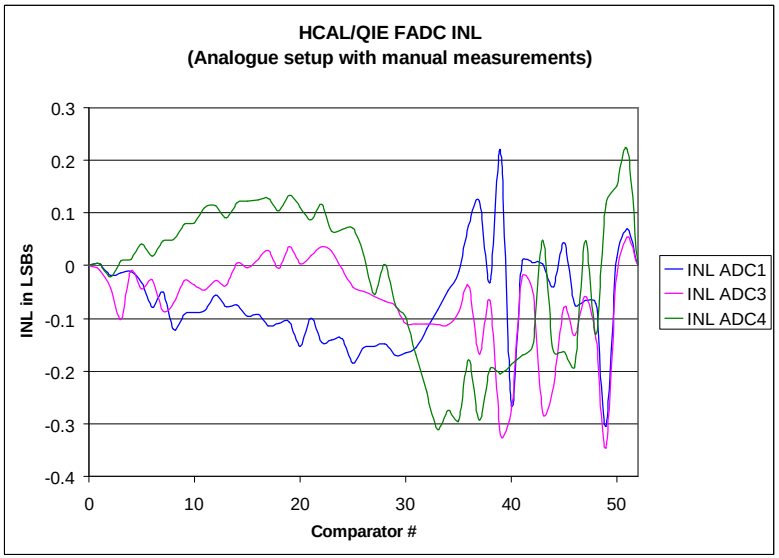
FLASH ADC Quantization

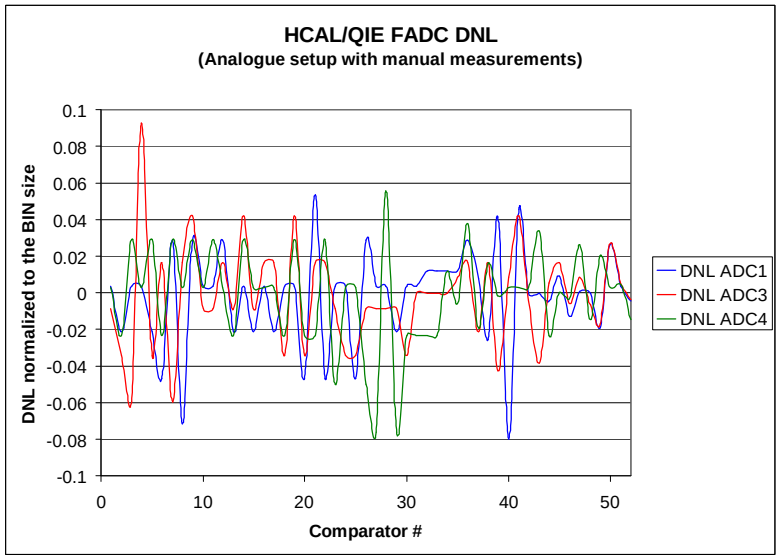


QIE Status

QIE ASIC

- Current splitter design submitted and tested
- Input amplifier with polarity and gain adjust submitted and tested
- Non-linear Flash ADC design submitted and tested
- **Full design submitted – back mid to late June '01**





QIE Schedule

Task Name	Start	Finish	Duration
AMS splitter test chip	Mon 11/2/98	Fri 4/30/99	130 days
Test Splitter	Mon 8/30/99	Fri 10/29/99	45 days
RAD Testing	Mon 11/1/99	Fri 3/3/00	90 days
AMP w/ polarity and gain adjust	Mon 6/28/99	Fri 10/1/99	70 days
FAB AMP w/ polarity and gain adjus	Mon 10/4/99	Fri 4/14/00	140 days
Test AMP w/ polarity and gain adjus	Mon 5/29/00	Fri 6/30/00	25 days
ADC for 4 range splitter	Mon 8/30/99	Fri 1/28/00	110 days
FAB ADC for 4 range Splitter	Tue 2/1/00	Mon 5/15/00	75 days
Test ADC for 4 range splitter	Mon 7/3/00	Fri 8/11/00	30 days
New Amp	Mon 2/28/00	Fri 3/31/00	25 days
FAB new Amp	Mon 4/3/00	Fri 7/14/00	75 days
Test new Amp	Mon 7/31/00	Fri 9/1/00	25 days
Full CMS QIE Design	Mon 3/27/00	Mon 3/5/01	246 days
FAB Full CMS QIE	Mon 3/5/01	Fri 6/15/01	75 days
Test Full CMS QIE	Mon 7/2/01	Fri 8/24/01	40 days
Mod Full CMS QIE	Mon 7/16/01	Fri 10/19/01	70 days
FAB Eng/Prod Run	Mon 10/22/01	Fri 2/1/02	75 days
Test Eng/Prod Run	Mon 2/4/02	Fri 3/15/02	30 days
PROD Mods	Mon 3/18/02	Fri 4/12/02	20 days
PROD Fab	Mon 4/15/02	Fri 7/26/02	75 days
Production Contingency	Mon 7/29/02	Fri 11/8/02	75 days

Channel Control ASIC

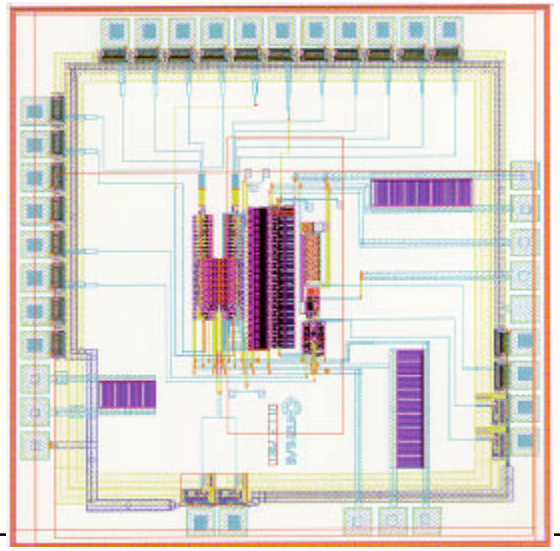
The CCA provides the following functions:

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to "reset" the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

CCA Status

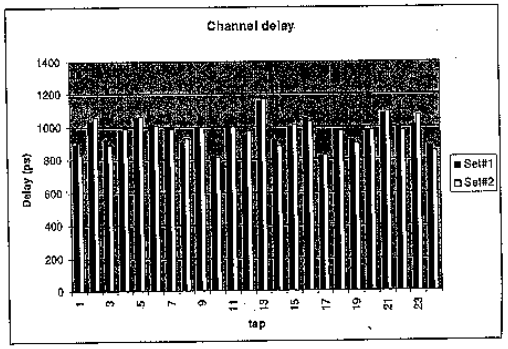
Channel Control ASIC

- DLL for timing control submitted and tested
- 1ns multiplexer design submitted and tested
- Serial Interface design submitted and tested
- **Full design will be submitted at end of June**



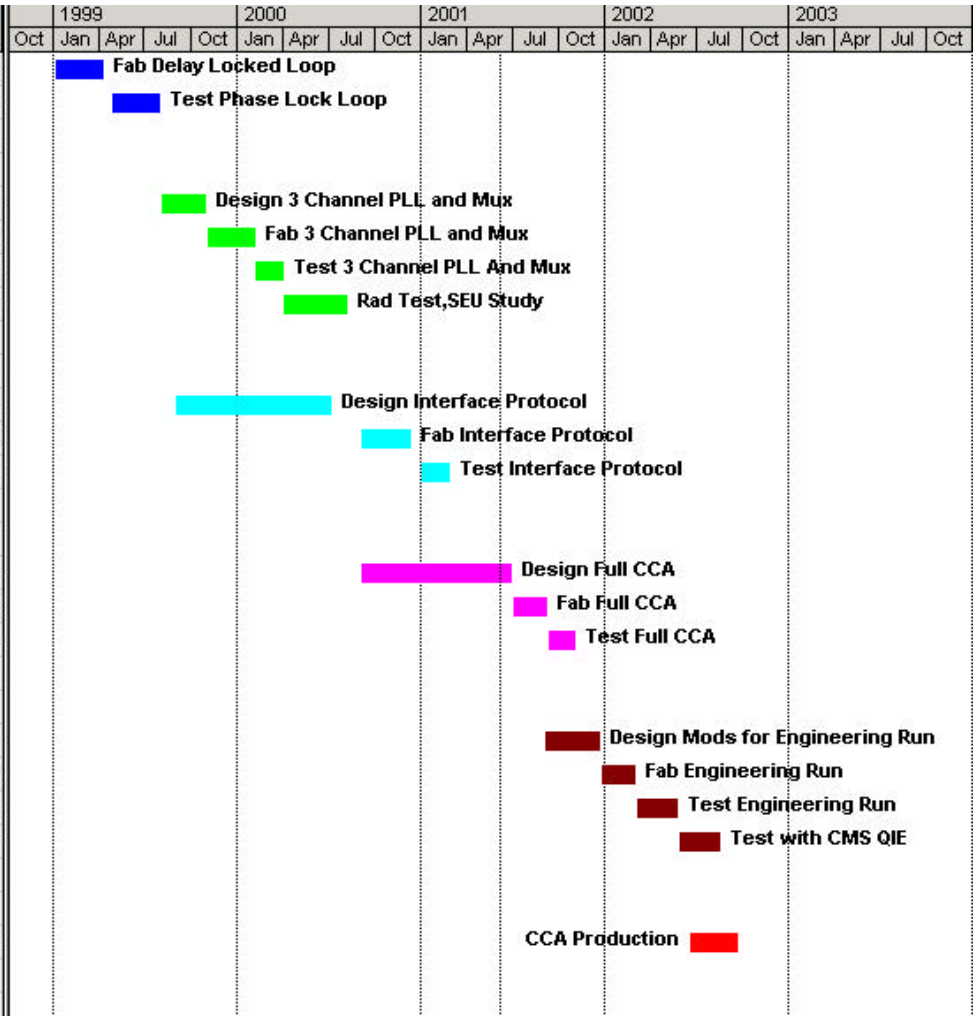
Measured delays vs. tap

- Average delay : 972p STD : 77ps
- Min delay : 810p
- Max delay : 1170p



CCA Schedule

Task Name	Start	Finish	Duration
Fab Phase Locked Loop	Mon 1/4/99	Fri 4/9/99	70 days
Test Phase Lock Loop	Mon 4/26/99	Fri 7/30/99	70 days
Design 3 Channel PLL and	Mon 8/2/99	Fri 10/29/99	65 days
Fab 3 Channel PLL and Mu	Mon 11/1/99	Fri 2/4/00	70 days
Test 3 Channel PLL And M	Mon 2/7/00	Fri 3/31/00	40 days
Rad Test, SEU Study	Mon 4/3/00	Fri 8/4/00	90 days
Design Interface Protocol	Tue 8/31/99	Mon 7/3/00	220 days
Fab Interface Protocol	Mon 9/4/00	Fri 12/8/00	70 days
Test Interface Protocol	Mon 1/1/01	Fri 2/23/01	40 days
Design Full CCA	Mon 9/4/00	Fri 6/29/01	215 days
Fab Full CCA	Mon 7/2/01	Fri 9/7/01	50 days
Test Full CCA	Mon 9/10/01	Fri 11/2/01	40 days
Design Mods for Engineeri	Mon 9/3/01	Fri 12/21/01	80 days
Fab Engineering Run	Mon 12/24/01	Fri 3/1/02	50 days
Test Engineering Run	Mon 3/4/02	Fri 5/24/02	60 days
Test with CMS QIE	Mon 5/27/02	Fri 8/16/02	60 days
CCA Production	Mon 6/17/02	Fri 9/20/02	70 days



GOL Design Specifications

Synchronous (constant latency)

Transmission speed

- **fast: 1.6 Gbps , 32 bit data input @ 40 MHz**
- **slow: 0.8 Gbps , 16 bit data input @ 40 MHz**

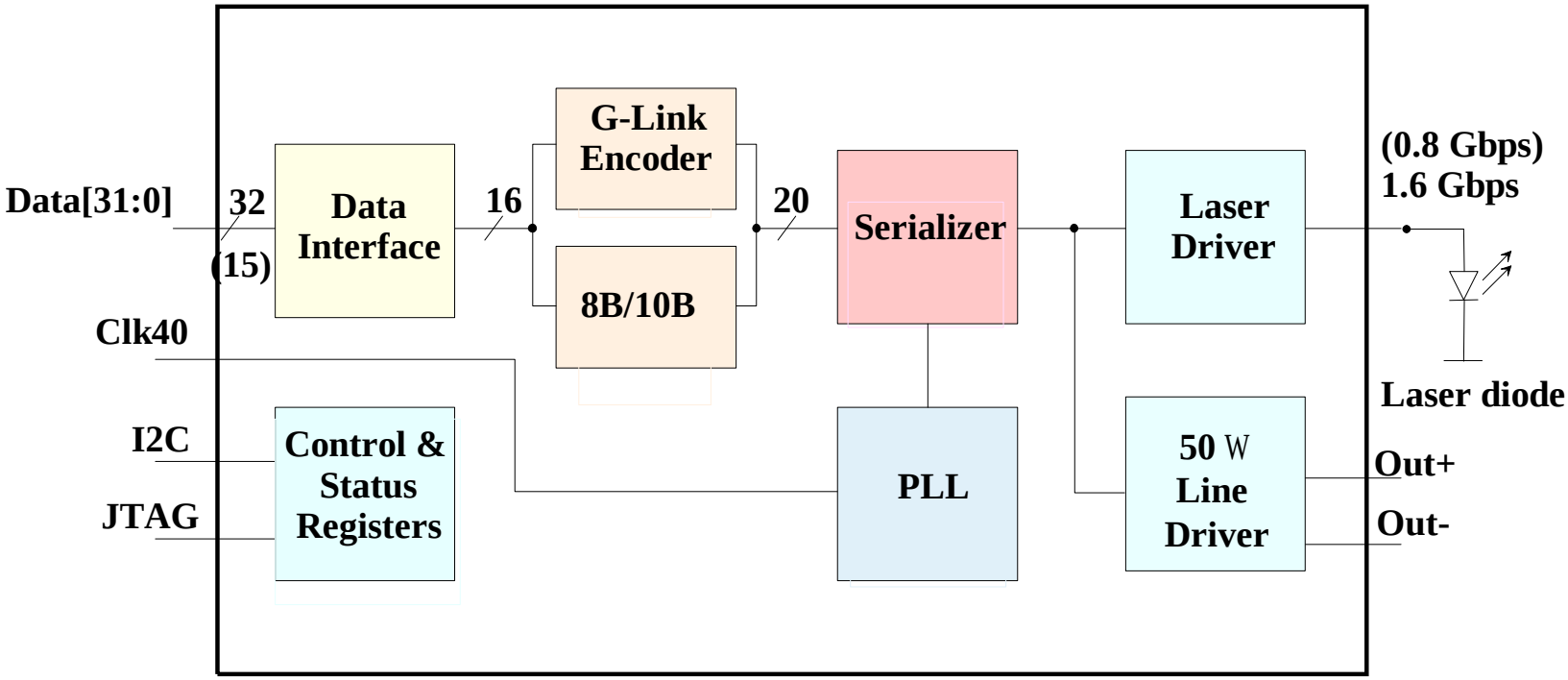
Two encoding schemes

- **G-Link**
- **Fiber channel (8B/10B)**

Interfaces for control and status registers

- **I2C**
- **JTAG**

Gigabit link (G-Link, 8B/10B optional)



GOL Radiation hardness

Deep submicron (0.25 um) CMOS

Enclosed CMOS transistors

Triple voting in state machines

Up-sizing of PLL components

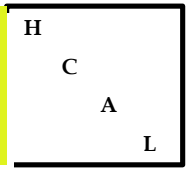
Auto-error correction in Config. registers

Single Event Upsets

- Can we extrapolate for LHC?

CMS Environment	Pixel R = 4 – 20cm	Endcap ECAL R = 50 – 130cm	Tracker R = 65-120cm	Cavern R = 700 – 1200cm
Error/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$
#chips for one error each hour!	71	5.3K	12K	32M

GOL Status



- **Bit error rate test in the 800Mbit/s G-Link mode: 20 hours error free transmission (external laser driver).**
- **Bit error rate test in the 1.6Gbit/s 8B/10B mode: 13 hours error free transmission (external laser driver).**
- **I2C interface successfully tested.**
- **JTAG interface successfully tested.**

- **Need to understand and fix jitter problem on internal laser driver. This will be fixed in the next submission (April '01).**

- **We are awaiting promised packaged parts (and waiting…….)**

Rad Tolerant Voltage Regulator

Developed by ST Microelectronics

Specified by CERN RD49

Shown to be Rad Hard

Presently fixing overvoltage protection

Pre-preduction parts due June 2001??

Production parts late 2001??

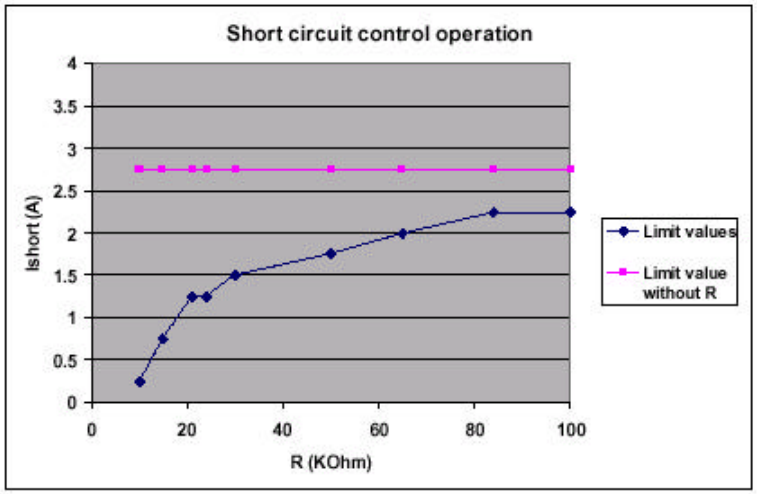
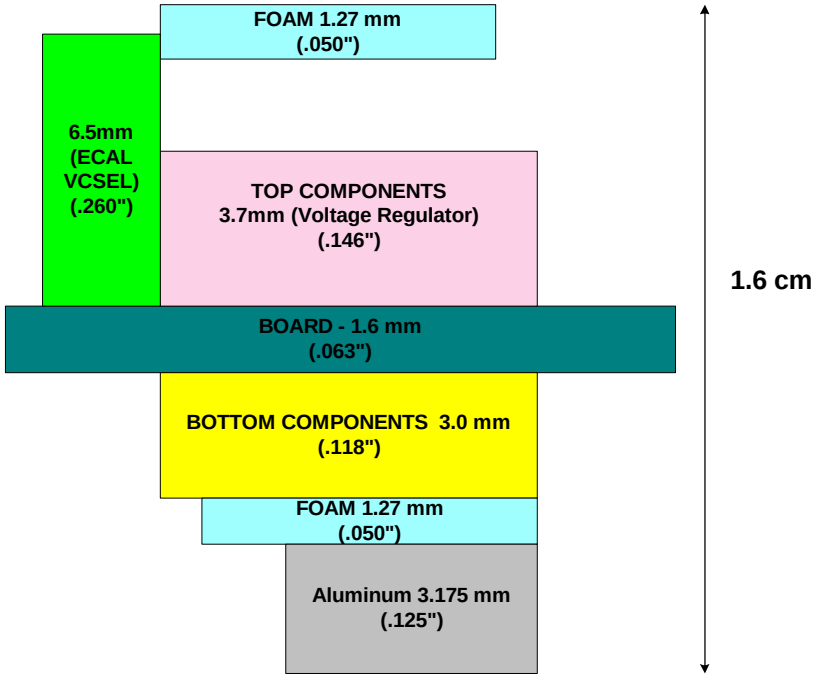


Fig. 7: Tuning of the maximum output current in a 2nd edition prototype regulator (version 2.5 V).

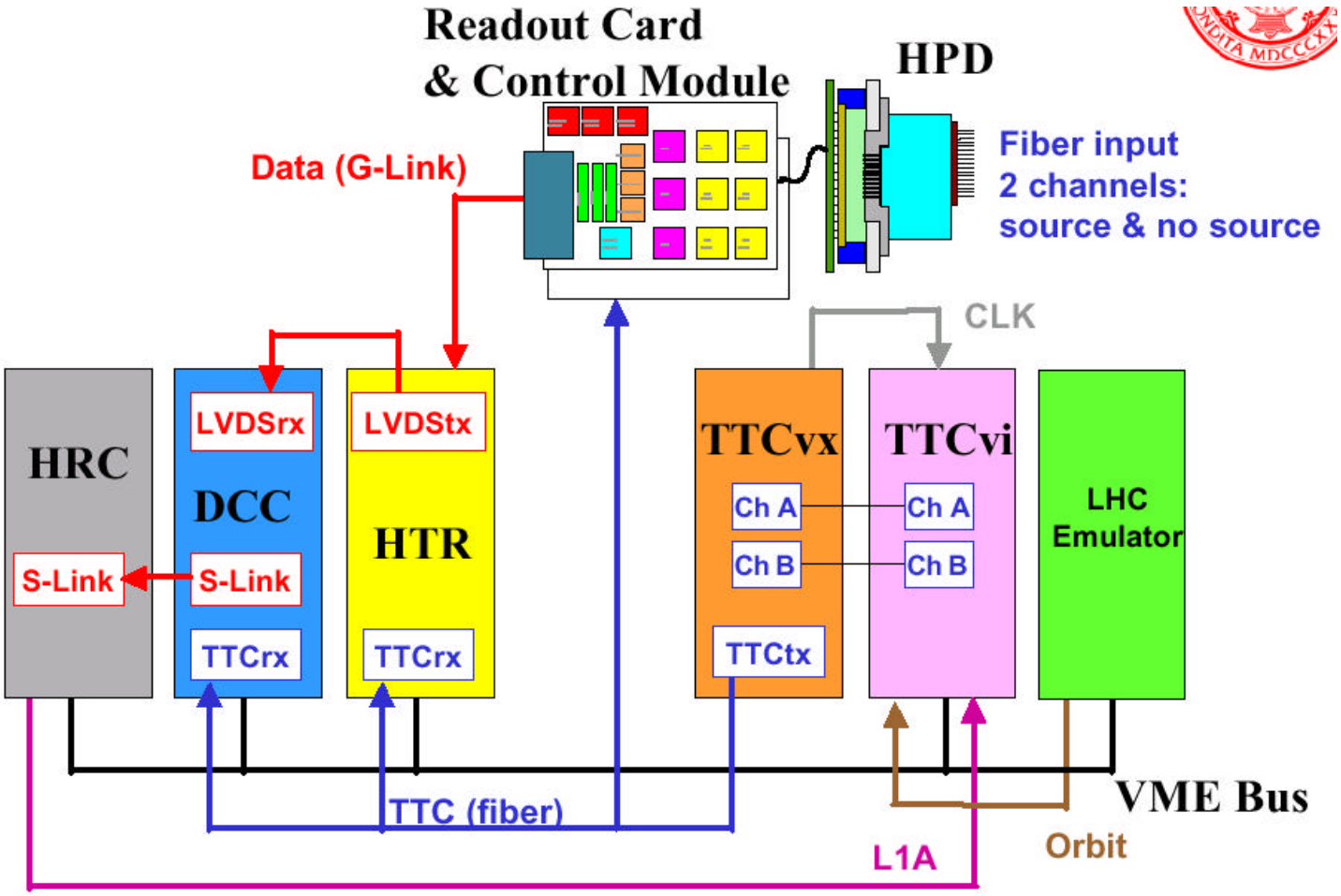
Readout Card Component Height

Goal is 1.6 cm stack



Geometric Space For Components

Plan for FE/HTR Integration



Summary

QIE Tests begin this month

FE/DAQ integration planned for this fall

- **2 channel FE card**
  - 2 QIEs
  - Commercial G-Link (@800 Mb/s)
- **6U HTR card**
- **9U DCC module**

Next – ready for summer 2002 test beam

- **6 channel FE card goals**
  - 6 QIEs
  - 3 Rad hard Voltage Regulators
  - 2 GOLs (8B/10B Encoding @1.6Gb/s)
  - Custom VCSEL package
  - 3 CCAs